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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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09/901,917

07/09/2001

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11675.101.1.1

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11/06/2003

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EXAMINER

THOMAS, TONIAE M

ART UNIT

PAPER NUMBER

2822

DATE MAILED: 11/06/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/901,917

Applicant(s)

WALKER ET AL.

Examiner

Toniae M. Thomas

Art Unit

2822

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 12 August 2003.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-23 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-23 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 09 July 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ 6) ☐ Other: _____

DETAILED ACTION

1. This Office action is an official response to the amendment filed on 12 August 2003. Currently, claims 1-23 are pending.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. *Claims 1, 2, 6, 9- 15, 17, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al. (US 5,343,354) in view of Wolf et al. (Silicon Processing for the VLSI Era – Vol. 1: Process Technology).*¹

The Lee et al. patent (Lee) discloses a process of forming a container cell (figs. 4A-4E and accompanying text). The process comprises the following steps: forming a trench 10 in a semiconductor substrate 100, the substrate having an upper surface (fig. 4A and col. 5, lines 8-16); forming a conformal isolation film 101 within the trench (fig. 4A and col. 5, lines 24-30); growing a gate oxide 1 on the upper surface of the substrate 100 (fig. 4B and col. 5, lines 54-57); forming a first gate stack upon the substrate and having an edge aligned with and adjacent to an edge of the trench (fig. 4B); forming a second gate stack upon the isolation film 101 (fig. 4B); etching a container cell 50 into

¹ The Lee et al. patent was relied upon in the previous Office action mailed.

Art Unit: 2822

the isolation film 101 (fig. 4C), the container cell 50 being situated substantially between the first and second gate stacks and having an edge defined by the substrate 100 and the isolation film 101 (fig. 4C), the edge of the container cell substantially extending to and terminating at each of the first and second gate stacks (fig. 4C), wherein the substrate and the isolation film have an interface that extends below the edge into the substrate (fig. 4C); and forming a storage node SE within the container cell (fig. 4D); forming a cell dielectric 20 upon the storage node (fig. 4E); and forming a cell plate PE upon the first gate stack, upon the cell dielectric, and upon the second gate stack (fig. 4E).²

A portion of the container cell extends beneath the first gate stack, as recited in claim 2 (fig. 4C).

The isolation film 101 is a BPSG film, as recited in claim 6 (col. 5, lines 24-30).

The method further comprises the following steps as recited in claim 9: forming a first polycrystalline silicon layer SE within the container cell (fig. 4D and col. 6, lines 28-35); depositing a cell dielectric 20 upon the first polycrystalline silicon layer (fig. 4E and col. 7, lines 3-5); and depositing a second polycrystalline silicon layer PE continuously upon the first gate stack, upon the cell dielectric, and upon the second gate stack (col. 7, lines 6-13), wherein the first polycrystalline layer forms the storage node and the second polycrystalline silicon layer forms the cell plate.

The isolation film 101 and the substrate 100 have an interface below the container cell 50, as recited in claim 12 (fig. 4C).

² See Appendix A.

The isolation film 101 and the substrate 100 have an interface below the container cell, such that the interface is coplanar with the edge defined by the substrate and the isolation film, as recited in claim 13 (fig. 4C). See also Appendix A.

The container cell is electrically isolated between the isolation film 101 and the substrate 100, as recited in claim 17 (fig. 4C).

The isolation film and the substrate have an interface below the container cell, such that the interface is not coplanar with the edge defined by the substrate and the isolation film, as recited in claim 14 (fig. 4C). See Appendix A.

Lee lacks anticipation in not teaching the following limitations: growing the gate oxide 1 such that it extends below the upper surface of the substrate; and forming the first and second polycrystalline silicon layers using an in-situ doping CVD process, as recited in claim 10 and 11.

The Wolf et al. reference [Wolf (Vol. 1)] discloses the use of thermally grown oxide as a gate oxide in MOS devices (page 198, lines 12-13). When thermal oxidation is used to form a gate oxide film on a semiconductor substrate, such as the substrate 100 of Lee, the gate oxide extends below the upper surface of the substrate.

Wolf (Vol. 1) also describes a method for forming doped polycrystalline silicon using an in-situ doping CVD process (page 182, lines 6-18).

Since Lee and Wolf (Vol. 1) are all from the same field of endeavor, the purpose disclosed by Wolf (Vol. 1) would have been recognized in the pertinent art of Lee.

One having ordinary skill in the art would have been motivated to modify Lee, at the time the invention was made, by [1] growing the gate oxide 1 using thermal oxidation such that it extends below the upper surface of the substrate and [2] forming the first and second polycrystalline silicon layers using an in-situ doping CVD process, as taught by Wolf (Vol. 1), for the following reasons: thermally grown oxide is of higher quality than an oxide film deposited using CVD; and in-situ doped polycrystalline silicon does not require a separate doping step.

3. *Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al. in view of Wolf et al. as applied to claims 1 and 15 above, and further in view of Lou et al. (US 5,872,045).*

Since the trench 10 is substantially vertical, it is inherent that the trench is formed using an anisotropic etch process.³ However, Lee does not teach that forming the trench comprises the steps of: spinning on a photoresist; masking, exposing, and patterning the photoresist to create a photoresist mask; and anisotropically etching through the photoresist mask.

The Lou et al. patent (Lou) discloses a method for forming an isolation trench (figs. 6, 7, 8A, 9-11 and accompanying text). The method comprises spinning on a photoresist; masking, exposing, and patterning the photoresist to create a photoresist

³ With anisotropic etching processes, etching occurs in a single direction.

mask 16 (fig. 6 and col. 4, lines 43-47),⁴ and anisotropically etching through the photoresist mask (fig. 6 and col. 4, lines 47-51). The photoresist mask 16 protects the active regions of the semiconductor substrate 10 during the etching process to form the isolation trench.

Since Lee, Wolf (Vol. 1), and Lou are all from the same field of endeavor, the purpose disclosed by Lou would have been recognized in the combination of Lee and Wolf (Vol. 1).

One having ordinary skill in the art would have been motivated to modify the combination of Lee and Wolf (Vol. 1), at the time the invention was made, to form the trench using the process taught by Lou, wherein the trench is formed by anisotropically etching through a patterned photoresist, since the patterned photoresist protects the active regions of the semiconductor substrate from damage during the etching process to form the trench.

4. *Claims 4, 5, 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al. in view of Wolf et al. as applied to claims 1 and 15 above, and further in view of Poon et al. (US 5,064,683).*

As previously discussed, Lee teaches that the isolation film 110 is BPSG (col. 5, lines 24-30). However, Lee does not teach that the isolation film is an oxide film formed

⁴ Lou refers to the steps of masking, exposing, and patterning as "conventional photolithographic techniques."

Art Unit: 2822

by the decomposition of TEOS, as recited in claims 4 and 16; or is a PSG film, as recited in claim 5.

The Poon et al. patent (Poon) describes a method for forming an isolation trench (figs. 1, 2, and col. 5, line 49 – col. 6, line 41). The method comprises forming a trench 14 in a semiconductor substrate 12, the substrate having an upper surface (fig. 1); and forming a conformal isolation film 20 within the trench (fig. 1), wherein the isolation film is one of the group comprising an oxide film formed by decomposing TEOS, a PSG film, and a BPSG film (col. 5, lines 58-62).

Since Lee, Wolf (Vol. 1), and Poon are all from the same field of endeavor, the purpose disclosed by Poon would have been recognized in the combination of Lee and Wolf (Vol. 1).

It would have been obvious to one having ordinary skill in the art, at the time the invention was made, to modify the combination of Lee and Wolf (Vol. 1) by forming the isolation film of either a PSG film or an oxide film formed by the decomposition of TEOS, as taught by Poon, because both PSG and TEOS silicon oxide are alternate materials that may be used in place of BPSG as the isolation film.

5. *Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al. in view of Wolf et al. as applied to claims 1 and 15 above, and further in view of Wolf (Silicon Processing for the VLSI Era – Vol. 3: The Submicron MOSFET).⁵*

⁵ The Wolf (Vol. 3) was relied upon in the Office action mailed on 28 March 2003.

Lee does not teach the step of forming a silicon nitride spacer upon the first and second gate stacks, as recited in claim 7.

Wolf (Vol. 3) describes a method for forming a MOS transistor, wherein the MOS transistor comprises a gate electrode, and silicon nitride spacers formed on the gate electrode (page 635, fig. 9-62(b)).

Since Lee, Wolf (Vol. 1), and Wolf (Vol. 3) are all from the same field of endeavor, the purpose disclosed by Wolf (Vol. 3) would have been recognized in the combination of Lee and Wolf (Vol. 1).

One having ordinary skill in the art would have been motivated to modify the combination of Lee and Wolf (Vol. 1), at the time the invention was made, by forming a silicon nitride spacer upon the first and second gate stacks, as taught by Wolf (Vol. 3), because silicon nitride spacers enhance the gate fringing field effects (Wolf (Vol. 3) – page 634, High Dielectric Spacers).

6. *Claims 8 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al. in view of Wolf et al. as applied to claims 1 and 15 above, and further in view of Wolf (Silicon Processing for the VLSI Era – Vol. 2: Process Integration).⁶*

Lee does not teach the step of using an RIE etch process to etch the container cell, as recited in claims 8 and 18.

Wolf (Vol. 2) discloses a method for forming a trench capacitor, wherein the trench is formed using RIE (page 602, Section 8.3.3.2 – first paragraph).

Since Lee, Wolf (Vol. 1), and Wolf (Vol. 2) are all from the same field of endeavor, the purpose disclosed by Wolf (Vol. 2) would have been recognized in the combination of Lee and Wolf (Vol. 1).

One having ordinary skill in the art would have been motivated to modify the combination of Lee and Wolf (Vol. 1), at the time the invention was made, by forming the container cell using an RIE process, as taught by Wolf (Vol. 2), because RIE is a controllable anisotropic etch process.

7. *Claims 19-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al. in view of Wolf et al. (Vol. 1) and Lou et al.*

Again, Lee discloses a process of forming a container cell (fig. 4A-4E). The method comprises the following steps as discussed above with respect to claims 1, 15, and 23: forming a trench 10 in a semiconductor substrate 100, the substrate having an upper surface (fig. 4A); forming a conformal isolation film 101 within the trench by forming an oxide film by deposition (fig. 4A and col. 5, lines 24-30); growing a gate oxide 1 on the upper surface of the substrate (fig. 4B); forming a first gate stack upon the substrate and having an edge aligned with and adjacent to an edge of the trench (fig. 4B); forming a second gate stack upon the isolation film within the trench (fig. 4B); and etching a container cell 50 into the isolation film within the trench, the container cell being situated substantially between the first and second gate stacks and having an edge defined by the substrate and the isolation film (fig. 4C), the edge of the container

⁶ The Wolf (Vol. 2) reference was relied upon in the Office action mailed on 28 March 2003.

cell substantially extending to and terminating at each of the first and second gate stacks (fig. 4C), wherein the substrate and the isolation film form an interface that extends below the container cell into the substrate (fig. 4C).

The edge of the container cell and an interface between the isolation film and the substrate are coplanar, as recited in claim 20 (fig. 4C). See Appendix A.

The edge of the container cell and an interface between the isolation film and substrate are not coplanar, as recited in claim 21 (fig. 4C). See Appendix A.

The method further comprises: forming a first polycrystalline silicon layer SE within the container cell 50 (fig. 4D); depositing a cell dielectric 20 upon the first polycrystalline silicon layer (fig. 4E); and depositing a second polycrystalline silicon layer PE continuously upon the first gate stack, upon the cell dielectric, and upon the second gate stack (fig. 4E).

As discussed above with respect to claims 1, 3, 15, and 23, Lee does not teach the following steps: forming the trench 10 by spinning on a photoresist, masking, exposing and patterning the photoresist to create a photoresist mask, and anisotropically etching through the photoresist mask; and growing the gate oxide such that it extends below the upper surface of the substrate.

As discussed previously, Wolf (Vol. 1) discloses the use of thermally grown oxide as a gate oxide in MOS devices (page 198, lines 12-13). When thermal oxidation is used to form a gate oxide film on a semiconductor substrate, such as the substrate 100 of Lee, the gate oxide extends below the upper surface of the substrate.

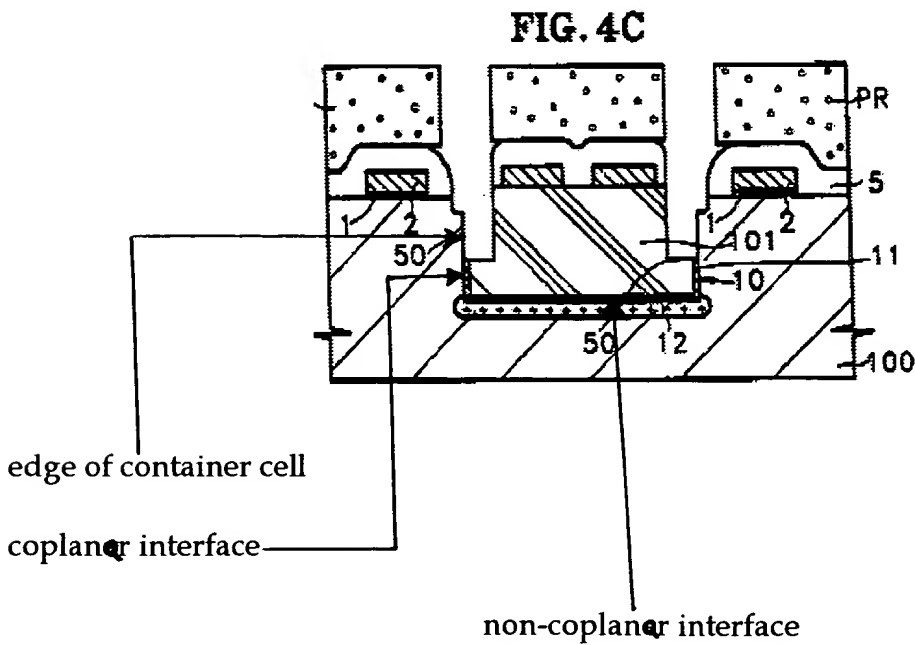
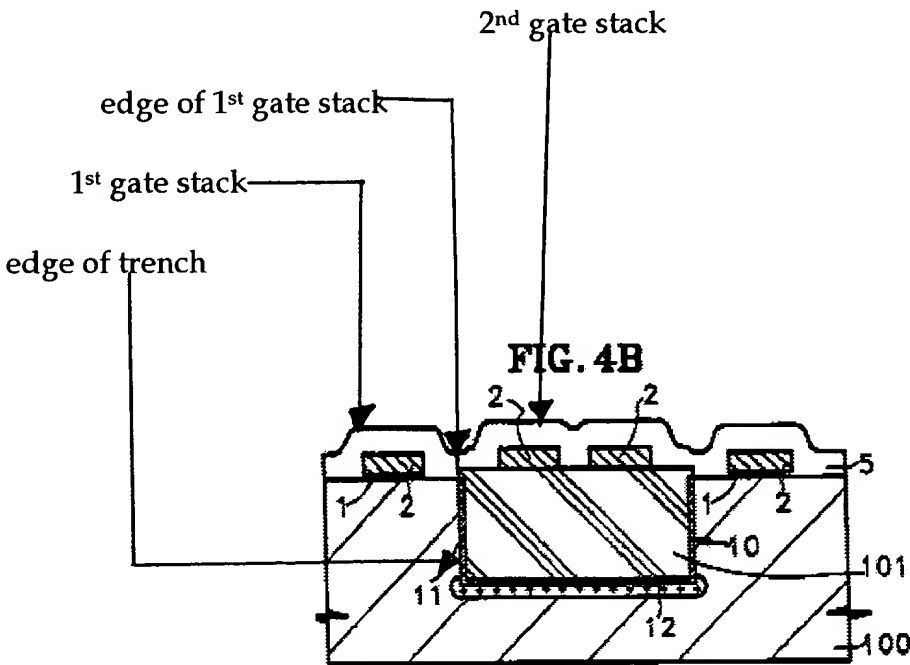
As discussed previously, Lou discloses a method for forming an isolation trench (figs. 6, 7, 8A, 9-11 and accompanying text). The method comprises spinning on a photoresist; masking, exposing, and patterning the photoresist to create a photoresist mask 16 (fig. 6 and col. 4, lines 43-47); and anisotropically etching through the photoresist mask (fig. 6 and col. 4, lines 47-51). The photoresist mask 16 protects the active regions of the semiconductor substrate 10 during the etching process to form the isolation trench.

To provide a gate oxide having a higher quality than an oxide film deposited using CVD, and to protect the active regions of the substrate from damage during the etching process to form the trench, one having ordinary skill in the art would have been motivated to modify Lee, at the time the invention was made, by: [1] growing the gate oxide 1 using thermal oxidation, as taught by Wolf (Vol. 1), and [2] forming the trench such that the substrate is anisotropically etched through a patterned photoresist, as taught by Lou.

Response to Arguments

8. Applicant's arguments, see page 9, line 6 to page 10, line 8, filed 12 August 2003, with respect to claims 1-23 have been fully considered and are persuasive. The objection to the specification and the rejection of claims 1-23 under 35 USC §112, first paragraph has been withdrawn.

Appendix A



Art Unit: 2822

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Toniae M. Thomas whose telephone number is (703) 305-7646. The examiner can normally be reached on Monday through Thursday from 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (703) 308-4905. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

TMJ

30 October 2003


AMIR ZARABIAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800